

THE INVENTION CLAIMED IS:

sub A1 1. An apparatus adapted to multiplex debug signals of an integrated circuit, the apparatus comprising:

at least a first multiplexing circuit and a second multiplexing circuit, wherein:

the first multiplexing circuit is adapted to receive first debug signals from an integrated circuit and to selectively multiplex at least a first portion of the first debug signals onto a first bus; and

the second multiplexing circuit is adapted to receive second debug signals from the integrated circuit and to selectively multiplex at least a first portion of the second debug signals onto a second bus;

a logic circuit adapted to combine any debug signals of the first bus and any debug signals of the second bus onto a third bus; and

an output stage adapted to selectively output debug signals of the third bus.

2. The apparatus of claim 1 wherein the output stage comprises a third multiplexing circuit adapted to receive debug signals of the third bus and to selectively multiplex the debug signals onto a fourth bus.

3. The apparatus of claim 2 wherein the third multiplexing circuit comprises:

a multiplexer adapted to receive the debug signals of the third bus and to selectively multiplex the debug signals onto the fourth bus; and

a control register coupled to the multiplexer and adapted to control multiplexing of debug signals by the

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4. The apparatus of claim 3 further comprising:
at least a first latch set coupled to the
third bus and adapted to latch debug signals from the third
bus at a first clock frequency and to output the latched
debug signals to the multiplexer.

5. The apparatus of claim 1 wherein the first, second and third buses are equally sized.

6. The apparatus of claim 1 wherein the logic circuit performs a bit-by-bit OR operation.

7. The apparatus of claim 1 wherein the first and second multiplexing circuits are adapted to multiplex on a nibble basis.

8. The apparatus of claim 1 wherein the first multiplexing circuit is part of a first partition of the integrated circuit adapted to selectively multiplex the first debug signals of the integrated circuit and wherein the second multiplexing circuit is part of a second partition of the integrated circuit adapted to selectively multiplex the second debug signals.

9. The apparatus of claim 8 wherein the first multiplexing circuit comprises:

a first multiplexer adapted to receive the first debug signals from the integrated circuit and to selectively multiplex at least the first portion of the

6 first debug signals; and

7 a first control register coupled to the first
8 multiplexer and adapted to control multiplexing of the first
9 debug signals by the first multiplexer; and

10 wherein the second multiplexing circuit
11 comprises:

12 a second multiplexer adapted to receive
13 the second debug signals from the integrated circuit and to
14 selectively multiplex at least the first portion of the
15 second debug signals; and

16 a second control register coupled to the
17 second multiplexer and adapted to control multiplexing of
18 the second debug signals by the second multiplexer.

10. The apparatus of claim 9 further comprising:
1 a first latch set coupled to the first
2 multiplexer and adapted to latch debug signals output by the
3 first multiplexer at a first clock frequency; and

4 a second latch set coupled to the second
5 multiplexer and adapted to latch debug signals output by the
6 second multiplexer at a second clock frequency.

11. The apparatus of claim 1 wherein the first
2 and second multiplexing circuits are part of a single
3 partition of the integrated circuit adapted to selectively
4 multiplex the first and second debug signals.

12. The apparatus of claim 11 wherein the first
2 multiplexing circuit comprises:

3 a first multiplexer adapted to receive the
4 first debug signals from the integrated circuit and to

5 selectively multiplex at least the first portion of the
6 first debug signals; and

7 a first control register coupled to the first
8 multiplexer and adapted to control multiplexing of the first
9 debug signals by the first multiplexer; and

10 wherein the second multiplexing circuit
11 comprises:

12 a second multiplexer adapted to receive
13 the second debug signals from the integrated circuit and to
14 selectively multiplex at least the first portion of the
15 second debug signals; and

16 a second control register coupled to the
17 second multiplexer and adapted to control multiplexing of
18 the second debug signals by the second multiplexer.

19 13. The apparatus of claim 12 further comprising:

20 a first latch set coupled to the first
21 multiplexer and adapted to latch debug signals output by the
22 first multiplexer at a first clock frequency; and

23 a second latch set coupled to the second
24 multiplexer and adapted to latch debug signals output by the
25 second multiplexer at a second clock frequency.

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A2 14. An apparatus adapted to multiplex debug
27 signals of an integrated circuit, the apparatus comprising:
28 at least a first multiplexing circuit and a
29 second multiplexing circuit, wherein:

30 the first multiplexing circuit is
31 adapted to receive first debug signals from an integrated
32 circuit and to selectively multiplex at least a first
33 portion of the first debug signals onto a first bus; and

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the second multiplexing circuit is
adapted to receive second debug signals from the integrated
circuit and to selectively multiplex at least a first
portion of the second debug signals onto a second bus;
a logic circuit adapted to combine any debug
signals of the first bus and any debug signals of the second
bus onto a third bus; and
a third multiplexing circuit adapted to
receive debug signals of the third bus and to selectively
multiplex the debug signals onto a fourth bus.

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15. A method of multiplexing debug signals of an
integrated circuit, the method comprising:
receiving first debug signals from an
integrated circuit;
selectively multiplexing at least a first
portion of the first debug signals onto a first bus;
receiving second debug signals from the
integrated circuit;
selectively multiplexing at least a first
portion of the second debug signals onto a second bus;
combining any debug signals of the first and
second buses onto a third bus; and
selectively outputting debug signals of the
third bus.

16. The method of claim 15 wherein selectively
outputting debug signals of the third bus comprises
selectively multiplexing the debug signals onto a fourth
bus.

1 *sub A2* 17. The method of claim 16 further comprising
2 *cont'd* latching at least a portion of the debug signals of the
3 third bus at one or more clock frequencies prior to
4 selectively multiplexing the debug signals onto the fourth
5 bus.

Sub B7 18. The method of claim 15 wherein the first,
2 second and third buses are equally sized.

1 *sub A3* 19. The method of claim 15 wherein combining any
2 debug signals of the first and second buses onto a third bus
3 comprises performing a bit-by-bit OR operation.

Sub B7 20. The method of claim 15 wherein selectively
2 multiplexing is performed on a nibble basis.

1 *sub A4* 21. The method of claim 15 wherein the step of
2 selectively multiplexing at least a first portion of the
3 first debug signals onto a first bus is performed by a first
4 partition of the integrated circuit; and

5 wherein selectively multiplexing at least a
6 first portion of the second debug signals onto a second bus
7 is performed by a second partition of the integrated
8 circuit.

Sub B7 22. The method of claim 21 further comprising:
latching the first portion of the first debug
3 signals at a first clock frequency following multiplexing of
4 the first portion of the first debug signals; and
5 latching the first portion of the second
6 debug signals at a second clock frequency following

7 multiplexing of the first portion of the second debug
8 signals.

1 ^{sub A5} 23. The method of claim 15 wherein the steps of
2 selectively multiplexing at least a first portion of the
3 first debug signals onto a first bus and selectively
4 multiplexing at least a first portion of the second debug
5 signals onto a second bus are performed by a single
6 partition of the integrated circuit.

1 24. A method of multiplexing debug signals of an
2 integrated circuit, the method comprising:
3 receiving first debug signals from an
4 integrated circuit;
5 selectively multiplexing at least a first
6 portion of the first debug signals onto a first bus;
7 receiving second debug signals from the
8 integrated circuit;
9 selectively multiplexing at least a first
10 portion of the second debug signals onto a second bus;
11 combining any debug signals of the first and
12 second buses onto a third bus; and
13 selectively multiplexing the debug signals
14 onto a fourth bus.

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